CLAIMS

What is claimed is

1. A method comprising maintaining speculative branch data for in-flight branches in a speculative branch target buffer (SBTB) cache by speculatively allocating a branch entry in a line of the SBTB after decoding an instruction containing a branch, speculatively updating branch data associated with the branch entry after branch prediction has been completed for the branch, and correcting the branch data after the branch has been executed.

2. The method of claim 1, wherein the branch data includes a speculative history field representing the speculative taken or not-taken history of the branch for a predetermined window of executions of the branch, and wherein said speculatively updating branch data comprises updating the speculative history field to reflect the taken or not-taken status of its most recent execution.

3. The method of claim 1, wherein the line has a corresponding a pattern table, and wherein said speculatively updating branch data comprises updating the pattern table.

4. The method of claim 1, wherein the branch comprises a conditional branch.

5. The method of claim 1, wherein the branch comprises a return from a subroutine.

6. The method of claim 1, wherein the branch comprises a call to a subroutine.

7. The method of claim 1, wherein the branch comprises an unconditional branch.

8. A method comprising:

speculatively allocating a first branch entry for a conditional branch in a speculative branch target buffer (SBTB) prior to execution of the conditional branch responsive to decoding the conditional branch and finding no branch entry in an architectural branch target buffer (ABTB) corresponding to the conditional branch;

speculatively allocating a second branch entry for the conditional branch in a the SBTB responsive to a subsequent failed attempt to locate a branch entry in the ABTB corresponding to the conditional branch;

allocating a third branch entry for the conditional branch in the ABTB after retirement of the conditional branch; and

subsequently performing branch prediction for the conditional branch by determining a predicted target address branch based upon branch data associated with the second branch entry.

9. The method of claim 8, further comprising speculatively updating branch data associated with the first branch entry after said performing branch prediction for the conditional branch.

10. A branch prediction circuit comprising:

speculative branch target buffer (SBTB) means for maintaining speculative branch data associated with in-flight branches;

architectural branch target buffer (ABTB) means, coupled to the SBTB means, for maintaining architectural branch data for branches corresponding to retired instructions; and

target address generation means coupled to both the SBTB means and the ABTB means for determining a predicted target address based upon the speculative branch data and the architectural branch data.

11. The branch prediction circuit of claim 10, wherein the SBTB means comprises a FIFO having entries corresponding to each of a plurality of pipeline stages of a microprocessor instruction pipeline.

12. The branch prediction circuit of claim 10, wherein the SBTB means includes a single read port and a single write port.

13. The branch prediction circuit of claim 10, wherein the SBTB means comprises a single-ported memory.

14. A machine-readable medium having stored thereon data representing sequences of instructions, the sequences of instructions which, when executed by a processor, cause the processor to:

speculatively allocate a first branch entry for a conditional branch in a speculative branch target buffer (SBTB) prior to execution of the conditional branch responsive to decoding the conditional branch and finding no branch entry in an architectural branch target buffer (ABTB) corresponding to the conditional branch;

speculatively allocate a second branch entry for the conditional branch in a the SBTB responsive to a subsequent failed attempt to locate a branch entry in the ABTB corresponding to the conditional branch;

allocate a third branch entry for the conditional branch in the ABTB after retirement of the conditional branch; and

subsequently perform branch prediction for the conditional branch by determining a predicted target address branch based upon branch data associated with the second branch entry.

15. The machine-readable medium of claim 14, wherein the sequences of instructions further cause the processor to speculatively update branch data associated with the first branch entry after said performing branch prediction for the conditional branch.

16. A branch prediction circuit comprising:

a speculative branch target buffer (SBTB) cache having a plurality of branch entries to maintain speculative branch data associated with in-flight branches, the speculative branch data including a speculative history of taken/not-taken outcomes associated with the in-flight branches; and

an architectural branch target buffer (ABTB) cache, coupled to the SBTB cache, the ABTB cache having a plurality of branch entries to maintain architectural branch data including the actual taken/not-taken outcomes associated with retired conditional branches.

17. The branch prediction circuit of claim 16, wherein the SBTB cache comprises a FIFO having entries corresponding to each of a plurality of pipeline stages of a microprocessor instruction pipeline.

18. The branch prediction circuit of claim 16, wherein the SBTB cache is dual-ported.

19. The branch prediction circuit of claim 16, wherein the SBTB cache is single-ported.

20. The branch prediction circuit of claim 16, wherein the ABTB cache is single-ported.

21. A processor comprising:

a fetch unit to speculatively retrieve instruction data for processing by an instruction pipeline; and

a branch prediction circuit, coupled to the fetch unit, to predict final target addresses for branch instructions contained within the instruction data, the branch prediction circuit including

a speculative branch target buffer (SBTB) cache having a plurality of branch entries to maintain speculative branch data associated with in-flight branches, the speculative branch data including a speculative history of taken/not-taken outcomes associated with the in-flight branches, and

an architectural branch target buffer (ABTB) cache, coupled to the SBTB cache, the ABTB having a plurality of branch entries to maintain architectural branch data including the actual taken/not-taken outcomes associated with retired conditional branches.

22. The processor of claim 21, wherein the SBTB cache comprises a FIFO having entries corresponding to each of a plurality of pipeline stages of the instruction pipeline.